IN THE CLAIMS:

Claims 2, 12, 13, 14, 15, 19, 20, 21, 24, 25, 26, 27 and 28 have been amended herein. All of the pending claims 1 through 30 are presented, pursuant to 37 C.F.R. §§ 1.121(c)(1)(i) and 1.121(c)(3), in clean form below. Please enter these claims as amended. Also attached is a marked-up version of the claims amended herein pursuant to 37 C.F.R. § 1.121(c)(1)(ii).

1. A method for forming a semiconductor wafer having an active surface, said active surface having bond pads thereon, the method comprising:
forming conductive traces over said active surface, each of said conductive traces having a first end, a second end, a top surface, and a bottom surface, said bottom surface of said first end of each said conductive trace being in contact with at least one of said bond pads;
forming a conductive bump on said top surface at said second end of said conductive traces, said conductive bump having a top portion transverse to said top surface of said conductive traces;
planarizing said top portion of said conductive bump;
forming a layer of encapsulation material to cover said active surface of said semiconductor wafer and to surround said conductive bump; and
reforming said conductive bump to a preplanarized shape extending above said layer.

A3 SUB B1 2. (Amended) The method of claim 1, wherein forming said conductive bump comprises placing a volume of solder paste on said at least one of said bond pads and reflowing said paste to form round balls.

3. The method of claim 1, wherein planarizing said top portion comprises compressing said top portion of said conductive bump with a platen.

4. The method of claim 1, wherein forming a layer of encapsulation material comprises at least partially overcoating said active surface of said semiconductor wafer and said conductive traces with a resin material.

5. The method of claim 1, wherein forming a layer of encapsulation material comprises at least partially overcoating said active surface of said semiconductor wafer and said conductive traces with a glass material.

6. The method of claim 1, wherein forming a layer of encapsulation material comprises placing said semiconductor wafer in a mold and injecting said encapsulation material into said mold.

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7. The method of claim 1, wherein reforming said conductive bump comprises reflowing said conductive bump to a substantially spherical shape.

8. The method of claim 1, wherein forming said conductive bump comprises depositing a conductive elastomer over said top surface at said second end of said conductive traces.

9. The method of claim 8, wherein planarizing said top portion comprises compressing said top portion of said conductive elastomer with a platen.

10. The method of claim 9, wherein reforming said conductive bump comprises removing said compression to permit said conductive elastomer to return to a precompressed shape.

11. The method of claim 1, further comprising dicing said semiconductor wafer to singulate at least one semiconductor die therefrom.

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12. (Amended) The method of claim 11, wherein said at least one singulated semiconductor die has a back and sides and further comprising forming a layer of encapsulation material on said semiconductor die to cover said back and said sides of said at least one singulated semiconductor die.

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13. (Amended) The method of claim 12, wherein forming said layer of encapsulation material on said back and sides of said at least one semiconductor die comprises overcoating said back and said sides of said at least one singulated semiconductor die and said conductive traces with a glass material.

14. (Amended) The method of claim 12, wherein forming said layer of encapsulation material on said back and sides of said at least one semiconductor die comprises overcoating said back and said sides of said at least one singulated semiconductor die and said conductive traces with a plastic material.

15. (Amended) The method of claim 12, wherein forming said layer of encapsulation material on said at least one semiconductor die comprises placing said at least one singulated semiconductor die into a second mold and injecting said encapsulation material into said second mold.

16. The method of claim 1, wherein said semiconductor wafer has a back surface and further comprising forming a layer of encapsulation material over said back surface to cover said back surface of said semiconductor wafer.

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17. The method of claim 16, wherein said layer of encapsulation material is formed over said back surface prior to reforming said conductive bump to a preplanarized shape.

18. The method of claim 16, wherein said layer of encapsulation material is formed over said back surface after reforming said conductive bump to a preplanarized shape.

19. (Amended) The method of claim 16, wherein forming said layer of encapsulation material over said back surface of said semiconductor wafer comprises overcoating said back surface of said semiconductor wafer with a glass material.

20. (Amended) The method of claim 16, wherein forming said layer of encapsulation material on said back surface of said semiconductor wafer comprises overcoating said back surface of said semiconductor wafer with a plastic material.

21. (Amended) The method of claim 16, wherein forming said layer of encapsulation material over said back surface of said semiconductor wafer further comprises placing said semiconductor wafer into a second mold and injecting said encapsulation material into said second mold.

22. The method of claim 1, wherein said semiconductor wafer is diced prior to reforming said conductive bump to a preplanarized shape.

23. The method of Claim 1, further comprising forming a chamfer between two or more bond pads on said active surface of said semiconductor wafer prior to forming said conductive bump.

24. (Amended) A method for forming an encapsulated semiconductor die having an active surface and bond pads on the active surface, the method comprising:

forming conductive traces over an active surface of a semiconductor wafer, each of said conductive traces having a first end, a second end, a top surface, and a bottom surface,

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said bottom surface of said first end of each said conductive trace being in contact with at least one bond pad on said active surface of said semiconductor wafer;

forming a conductive bump on said top surface at said second end of said conductive traces, said conductive bump having a top portion transverse to said top surface of said conductive traces;

planarizing said top portion of said conductive bump;

dicing said semiconductor wafer to singulate at least one semiconductor die;

forming a layer of encapsulation material on at least a portion of said active surface of said semiconductor die; and

reforming said conductive bump to a preplanarized shape extending above said layer.

25. (Amended) The method of claim 24, wherein said at least one singulated semiconductor die has a back and sides and further comprising forming said layer of encapsulation material on said semiconductor die to cover said back and said sides of said at least one semiconductor die.

26. (Amended) The method of claim 25, wherein forming said layer of encapsulation material on said back and sides of said at least one semiconductor die comprises overcoating said back and said sides of said at least one semiconductor die and said conductive traces with a glass material.

27. (Amended) The method of claim 25, wherein forming said layer of encapsulation material on said back and sides of said at least one semiconductor die comprises overcoating said back and said sides of said at least one semiconductor die and said conductive traces with a plastic material.

28. (Amended) The method of claim 25, wherein forming said layer of encapsulation material on said at least one semiconductor die comprises placing said at least one semiconductor die into a second mold and injecting said encapsulation material into said second mold.

29. The method of claim 24, wherein said semiconductor wafer is diced prior to reforming said conductive bump to a preplanarized shape.

30. The method of Claim 24, further comprising forming a chamfer between two or more bond pads on said active surface of said semiconductor wafer prior to forming said conductive bump.